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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,406	04/01/2005	John David Porter	12519-009US1	7508

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FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
BOKHARI, SYED M	
ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/510,406	PORTER ET AL.	
	Examiner	Art Unit	
	SYED BOKHARI	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant filed on August 1st, 2008 under has been entered. Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-8 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van der Putten et al. (US 6,327,273 B1) in view of Hayashi et al. (USP 5,062,124).

Van der Putten et al. discloses a wireless communication system for synchronizing the timing signals in the base stations with the following features: regarding claim 1, each module in the network having a clock of nominal frequency (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “transmitter and receiver modules include local clock each" recited in column 4 lines 10-21), that is not synchronized with the clocks of the other module(s) in the network (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “transmitter module reference clock and receiver modules reference clocks are not synchronized with each other” recited in column 4 lines 29-36 and lines 43-48), having a single input and one or more outputs of each module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “receiver module has one input and more than one output for data output and network clock output” recited in column 4 lines 16-21), where all the outputs are phase locked to each other but are not synchronized with

respect to the input (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the transmit clock signal and receive clock signal are synchronized, the receiving unit only has to become aware of the phase difference” recited in column 2 lines 45-53), means for determining the accumulated phase difference between the input clock and the output clock of each module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference value is determined” recited in column 2 lines 55-63 and column 3 lines 1-4), means for transmitting the accumulated phase difference to the terminating module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference value is determined and transmitted” recited in column 3 lines 4-5) and means for utilizing the received accumulated hose difference at the terminating module to lock the output clock at the terminating module to the input clock at the source module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the measured phase difference (P) is communicated to the receiver and used therein to generate a copy (CLK2)” recited in abstract lines 8-11, column 4 lines 37-43); regarding claim 2, in which the accumulated phase difference is transmitted at regular intervals in an ATM cell (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference is measured at the ATM, embedded and transmitted” recited in column 5 lines 53-62); regarding claim 3, the determining means comprises a first counter for counting clock cycles of the input signal clock, a second counter for counting

cycles of the output signal clock, and means for simultaneously reading the counts of the first and second counters (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “counter value is increased by one each time with clock cycle of input signal” recited in column 5 lines 58-67 and column 6 lines 1-3); regarding claim 5, the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counter (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase measurement device measures and transmits to the receiver” recited in column 5 lines 60-67 and column 6 lines 1-3); regarding claim 6, each module having a clock of nominal frequency (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “transmitter and receiver modules include local clock each" recited in column 4 lines 10-21), that is not synchronized with the clocks of the other module(s) (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “transmitter module reference clock and receiver modules reference clocks are not synchronized with each other” recited in column 4 lines 29-36 and lines 43-48), each module having a single input and one or more outputs (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “receiver module has one input and more than one output for data output and network clock output” recited in column 4 lines 16-21), where all the outputs are phase locked to each other but are not synchronized with respect to the input (Fig., a block diagram illustrating the segment of the network consisting of

transmitter and receiver modules, see “the transmit clock signal and receive clock signal are synchronized, the receiving unit only has to become aware of the phase difference” recited in column 2 lines 45-53), the method comprising the steps of determining the accumulated phase difference between the input clock and the output clock at each module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference value is determined” recited in column 2 lines 55-63 and column 3 lines 1-4), transmitting the determined accumulated phase difference to the terminating module (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference value is determined and transmitted” recited in column 3 lines 4-5), and utilizing the received accumulated phase difference at the terminating network to recover the clock at the source module of the network (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the measured phase difference (P) is communicated to the receiver and used therein to generate a copy (CLK2)” recited in abstract lines 8-11, column 4 lines 37-43); regarding claim 7, the accumulated phase difference is transmitted (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase difference is measured at the ATM, embedded and transmitted” recited in column 5 lines 53-62); regarding claim 8, applying the input clock of a module to a first counter within the, applying the output clock of the module to a second counter within the module and reading the counts of the first and second counters simultaneously at given intervals (Fig., a block diagram illustrating the segment

of the network consisting of transmitter and receiver modules, see “counter value is increased by one each time with clock cycle of input signal” recited in column 5 lines 58-67 and column 6 lines 1-3); regarding claim 11, comprises the steps of applying the input clock of a module to a first counter within the module, the determining means comprises a first counter for counting clock cycles of the input signal clock, a second counter for counting cycles of the output signal clock and means for simultaneously reading the counts of the first and second counters (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “counter value is increased by one each time with clock cycle of input signal” recited in column 5 lines 58-67 and column 6 lines 1-3); regarding claim 13, the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase measurement device measures and transmits to the receiver” recited in column 5 lines 60-67 and column 6 lines 1-3); regarding claim 14, the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see “the phase measurement device measures and transmits to the receiver” recited in column 5 lines 60-67 and column 6 lines 1-3); regarding claim 15, the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters (Fig., a block diagram illustrating the segment of the network

consisting of transmitter and receiver modules, see "the phase measurement device measures and transmits to the receiver" recited in column 5 lines 60-67 and column 6 lines 1-3); regarding claim 16, comprises the steps of applying the input clock of a module to a first counter within the module, applying the output clock of the module to a second counter within the module and reading the counts of the first and second counters simultaneously at given intervals (Fig., a block diagram illustrating the segment of the network consisting of transmitter and receiver modules, see "counter value is increased by one each time with clock cycle of input signal" recited in column 5 lines 58-67 and column 6 lines 1-3);

Van der Putten et al. do not disclose the following features: regarding claim 1, a packet switched communications system for transmitting synchronous data from a source module to a terminating module, over a network, the network comprising plurality of modules interconnected via transmission links; regarding claim 4, comprising a latch for storing the count of the counter counting the higher frequency clock and the count being clocked into the latch by an edge of the lower frequency clock; regarding claim 6, a method of recovering clock signals in a packet switched communications network the network comprising a plurality of modules interconnected via transmission links; regarding claim 12, comprising a latch for storing the count of the counter counting the higher frequency clock and the count being clocked into the latch by an edge of the lower frequency clock.

Hayashi et al. discloses a network synchronization system in a distributed

communication system with the following features: regarding claim 1 a packet switched communications system for transmitting synchronous data from a source module to a terminating module over a network, the network comprising plurality of modules interconnected via transmission links (Fig. 2, synchronizing communication devices, see "distributed communication system" recited in column 3 lines 41-48); regarding claim 4, comprising a latch for storing the count of the counter counting the higher frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 30-33) and the count being clocked into the latch by an edge of the lower frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 36-39); regarding claim 6, a method of recovering clock signals in a packet switched communications network the network comprising a plurality of modules interconnected via transmission links (Fig. 2, synchronizing communication devices, see "distributed communication system" recited in column 3 lines 41-48); regarding claim 8, applying the input clock of a module to a first counter within the module (Fig. 5, communication device, see "counter 43" recited in column 7 lines 10-16), applying the output clock of the module to a second counter within the module (Fig. 5, communication device, see "counter 43" recited in column 7 lines 17-25) and reading the counts of the first and second counters simultaneously at given intervals (Fig. 5, communication devices 11 and 12, see "selector 102" recited in column 8 lines 17-22 and lines 39-43); regarding claim 12, comprising a latch for storing the count of the counter counting the higher frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 30-33) and

the count being clocked into the latch by an edge of the lower frequency clock (Fig.4, node distribution, see "latch for store" recited in column 6 lines 36-39).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Van der Putten et al. by using the features, as taught by Hayashi et al., in order to provide a packet switched communications system for transmitting synchronous data from a source module to a terminating module, over a network, the network comprising plurality of modules interconnected via transmission links, a latch for storing the count of the counter counting the higher frequency clock, the count being clocked into the latch by an edge of the lower frequency clock, applying the input clock of a module to a first counter within the module. The motivation of using these functions is to enhance the system in a cost effective manner.

6. Claim 9-10 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van der Putten et al. (US 6,327,273 B1) in view of Hayashi et al. (USP 5,062,124) as applied to claims 6, 7, 8 and 16 above, and further in view of Rokugo (USP 5,864,248).

Van der Putten et al. and Hayashi et al. disclose the claimed limitations as describes the in paragraph 5 above. Van der Putten et al. and Hayashi et al. do not disclose the following features: regarding claim 9, in which step d) comprises transmitting the counts read in step f; regarding claim 10, or in which the counters are read on a transition of the lower frequency clock; regarding claim 17, in which step d)

comprises transmitting the counts read in step f); regarding claim 18, in which the counters are read on a transition of the lower frequency clock; regarding claim 19, in which the counters are read on a transition of the lower frequency clock and regarding claim 20, in which the counters are read on a transition of the lower frequency clock.

Rokugo discloses phase-locked loop circuit (PLL) for producing clock signals synchronized with transmitter in receiver with the following features: regarding claim 5, means for assembling an ATM cell containing the counts of the first and second counters (Fig. 9, phase synchronization system, see "time data 93" recited in column 1 lines 40-49); regarding claim 9, in which step d) comprises transmitting the counts read in step f (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40); regarding claim 10, or in which the counters are read on a transition of the lower frequency clock (Fig. 8, frequency response, see "data count value" recited in column 8, lines 46-52); regarding claim 17, in which step d) comprises transmitting the counts read in step f) (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40); regarding claim 18, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40); regarding claim 19, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40) and regarding claim 20, in which the counters are read on a transition of the lower frequency clock (Fig. 1, phase locked loop circuit, see "count value output from transmitter" recited in column 2 lines 22-40).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Van der Putten et al. with Hayashi et al. by using the features, as taught by Rokugo, in order to provide transmitting the counts, the counters are read on a transition of the lower frequency clock, in which the counters are read on a transition of the lower frequency clock and the counters are read on a transition of the lower frequency clock. The motivation of using these functions is to enhance the system in a cost effective manner.

Response to Arguments

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SYED BOKHARI whose telephone number is (571)270-3115. The examiner can normally be reached on Monday through Friday 8:00-17:00 Hrs..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang B. Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Syed Bokhari/
Examiner, Art Unit 2416
11/23/2008

/Kwang B. Yao/
Supervisory Patent Examiner, Art Unit 2416